Pre BondThrough Silicon Vias (TSVs) Testing in 3D ICs

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Abstract — **3-D Integrated Circuits (IC's) offer many advantages like higher device density, higher bandwidth, low-power, and smaller form-factor. Testing the integrity of interconnects realized by through silicon vias (TSVs) in 3-D integrated circuits (3-D IC) is considered a challenging task. TSVs are excessively small and fragile for current probe technology. Just like other components, the fabrication and bonding of TSVs can fail. A failed TSV can severely increase the cost and decrease the yield as the number of dies to be stacked increases. Author describes the on-die test architecture and probe technique needed for TSV testing, in which individual probe needles make contact with multiple TSVs at a time. Simulation results using LTSPICE are presented for a TSV network. It is demonstrated that one can achieve high resolution in these measurements and therefore high accuracy in defect detection when one or multiple TSVs at a time are targeted.**

Keywords: Integrated Circuits; Through silicon vias (TSVs); Die; Simulation.

I. INTRODUCTION

LOW power and high speed requirements keeps on pushing the semiconductor industry towards various innovative ideas and methodology. By doubling the number of transistors on a die every two years, chip makers have given us ever more powerful PCs and electronic gadgets at prices that shrink almost as fast as transistors do. So it may come as a surprise to many that today wires, not transistors, are determining the performance and cost of microchips [1]. Three Dimensional 3-D stacking technology has the potential to keep pace with the performance improvement projected by Moore's law. Three Dimensional Integrated circuits (3D IC's) reduce interconnects length by stacking multiple dies in a single package and smaller form factor. The length of global wires can be reduced by as much as 50%, wire-limited clock frequency can be increased by 3.9X, and wire-limited area can be decreased by 84% [2], [3]. Power can be reduced by 51% at the 45-nm technology node [3], [4]. In 3-D ICs, gates are placed in multiple dies, and the dies are stacked vertically on top of each other as illustrated in Figure 1. Since gates are distributed in multiple dies, the footprint area of each die of a 3-D IC becomes smaller than that of the circuit designed in 2-D. A smaller footprint area results in shorter total wirelength in 3-D ICs than in 2-D ICs [5], [6], [7]. Therefore, 3-D ICs have a high potential to improve the performance [7], [8], [9]. Shorter wirelength can also reduce interconnect power and improve routing congestion. Less routing congestion can in turn reduce the number of metal layers used for routing in each die of a 3-D IC, and the reduction of the metal layer count can contribute to cost reduction [10].

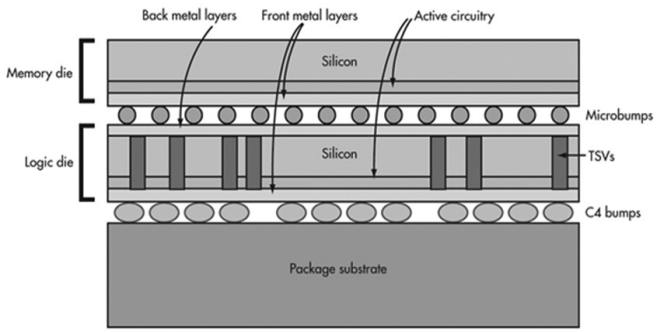

Figure 1. Cross-section of 3D IC.

II. THROUGH SILICON VIAS

A. Fabricating TSVs:

The functionality of 3-D integrated circuit (IC) strongly depends on the fidelity of signals through through-silicon vias (TSVs). A TSV is a vertical electrical connection passing through a silicon die. TSVs are copper vias with diameters that may range from 1 to 30 microns [11]. As the TSV process is not a perfect one, defects can be created while forming the TSVs before bonding (assuming a via-first process) or while bonding different dies together. The defect can be created by short through the oxide surrounding the TSVs resulting in finite resistance between TSV and substrate. The open defects or ruptures can also be created during TSV growth. The non-conformal growth of the insulator also creates defects or variation in TSV properties. At the post-bond stage, the defects can be created due to variation in the resistance of the bonding material or misalignment [12].

TSV testing can be separated into two distinct categories: pre-bond testing and post-bond testing. Pre-bond testing is directed to detecting defects that are inherent in the manufacture of the TSV itself, such as impurities or voids, while post-bond testing is directed to detecting faults caused by thinning, alignment, and bonding.

There are a number of pre-bond defects that can impact chip functionality. These include incomplete metal filling (or microvoids) in the TSVs, which increase resistance and path delay; partial breaks in the TSV, which result in a resistive path; and complete breaks in the TSV, which result in an open path. In addition, impurities in the TSV may also increase resistance and interconnect delay; and pinhole defects can lead to a leakage path to the substrate, with a corresponding increase in the capacitance between the TSV and the substrate. [13]

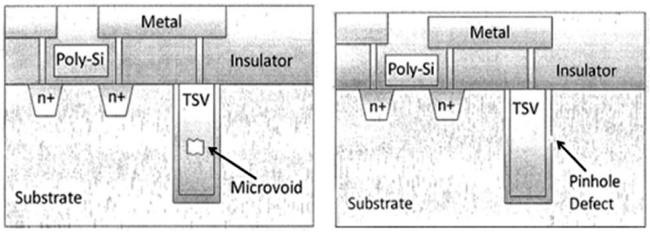

Figure 2*a*. Microvoid and Pinhole TSV defect.

Figure 2*a* illustrates a microvoid defect and a pinhole defect, respectively, of a TSV. A TSV is disposed in the substrate and can take the form of a metal pillar. The TSV may be formed by etching the substrate to form a deep via or trench, depositing a barrier material in the deep via or trench, and then depositing the material forming the TSV. When depositing the material forming the TSV in the deep via or trench, a microvoid, may occur in the TSV. This microvoid increases the resistance of the TSV. The pinhole defect may occur from uneven forming of the barrier material and causes leakage between the TSV and the substrate, increasing the TSV capacitance.

Various built-in self-test (BIST) methods have been proposed in the literature to address the challenges of test development for 3-D ICs [14], [15]. Implementation of BIST for a large number of TSVs requires a considerable die area. Current

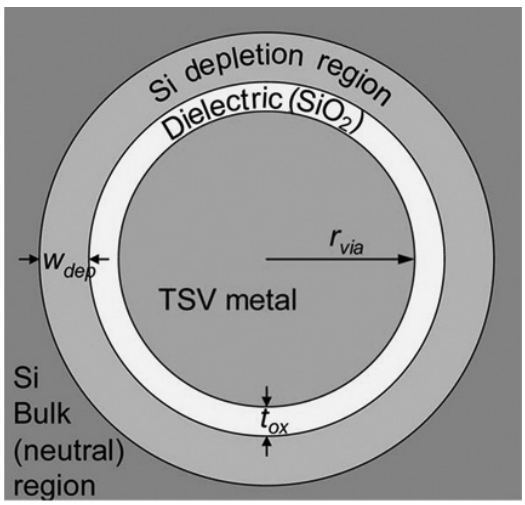

Figure 2*b*. Top cross-sectional view of a TSV surrounded by the dielectric (SiO2), the Si depletion region, and the bulk Si.

probe technology using cantilever or vertical probes requires a minimum pitch of 35μm.

They exert excessive vertical force on contact surface causing scrub marks and structural deformation. Moreover, they require large contact pads added to TSVs to ensure the connectivity [16]. A flexible membrane probe card with embedded metal probes has been proposed in the literature to probe TSVs [17]. In [18], Noia and Chakrabarty presented a DFT method for prebond testing in which individual probe needles contact multiple TSVs that are shorted together to form a network of TSVs. In this method, the capacitance and resistance of each TSV in the TSV network are determined to identify faulty TSVs.

Author presents a low-overhead digital test structure based on scan flip-flops (FFs) that detects the resistive defects in TSVs. Scan flip-flops (FFs) is implemented with 32 nm predictive technology model (PTM) [19] to be close to simulation program with integrated circuit emphasis (SPICE). The proposed model is verified to be applicable to various device models such as 32 nm PTM high-*k*/metalgate model.

Testing of TSVs: One basic approach to 3D-IC testing involves performing a post-bond test after each die has been bonded to the stack. The goal is to test portions of the system that could have been damaged during the bonding process. Because it is not viable to "un-bond" a die subsequently found to be defective, one study [20] maintains that performing a separate pre-bond (i.e., standalone) test to identify a Known Good Die (KGD) for stacking is more cost-effective than relying solely on post-bond testing to identify a defective die that has already rendered the entire system defective.

However, the economics of pre-bond testing have yet to be fully characterized, and one of the key challenges is how to apply the KGD test. With the exception of the bottom die, no probe pads exist for pre-bond testing because all the I/Os are accessible only through TSVs topped by fine-pitch micro-bumps, which are arrayed on both sides of the die.

Standard probe equipment applies tests only on a single side and even state-of-the-art production systems do not meet the fine-pitch and I/O bandwidth requirements of 3D-ICs. Moreover, it is difficult to perform pre-bond tests without damaging the micro-bumps or deforming the thinned wafers [21].Efforts are underway to deliver probe systems that facilitate probing on fine-pitch micro-bumps. Rocking Beam Interposer (RBI) technology [22] in membrane probe cards improves probing accuracy and minimizes bond pad damage. Contactless probing [23] may also prove viable.

At this time, however, these solutions are still a work-in-progress for meeting 3D-IC probing requirements. Likewise,

the test challenges specifically related to the handling of thinned wafers and thinned dies remain formidable [21, 24], and in 2010, SEMI created a taskforce specifically to define requirements and develop standards for the reliable handling and shipping of thin wafers.

Although there are new failure mechanisms due to defects caused by wafer thinning and by TSV filling, alignment, and bonding, their fault effects appear to be the same as those encountered in two-dimensional (2D) designs. Therefore, conventional stuck-at and transition-delay automatic test pattern generation (ATPG) can be used or extended to test 3D-ICs. For example, slack-based transition delay tests that target small delay defects and bridging tests that target bridging faults are already in use today to meet ultra-high test quality requirements. With the advent of 3D-ICs that offer smaller form factors and higher performance than current 2D designs, these advanced tests—already available in Synopsys' TetraMAX ATPG product—become necessary for screening 3D systems. In addition, greater system complexity of 3D-ICs demands tighter control of dynamic power consumption, which differs pre-bond versus post-bond (since TSVs are used to distribute power up the stack in the latter case).

Advanced power management techniques, such as power-aware ATPG and power domain-based testing, are required to control power consumption and avoid false failures during 3D-IC testing. Power-aware ATPG generates patterns that limit both shift mode and capture mode power to functional levels based on a designer-specified power budget. Power domain-based test generates patterns in compliance with a design's functional power states to reduce both dynamic and leakage power and avoid IR-drop issues. These advanced capabilities in the Synopsys test solution already have been successfully deployed to limit false failures on the tester, and will be essential for managing power during testing of 3D-ICs, which are also susceptible to increased thermal density and thermal variation [8].

Extensions to existing test automation that address very specific 3D-IC testing requirements include the ability to insert and connect TSV ports and related logic in a design, and the ability to generate "loopback" tests that allow data to be applied to and captured from the TSV I/Os to verify their functionality during KGD testing. For TSV connectivity tests, TetraMAX ATPG uses "dynamic bridging" fault models to generate at-speed patterns that can target time-sensitive shorts between TSV I/Os.

IV. PROPOSED TESTING SCHEME OF TSV ARRAYS

Scan Chain Method: Figure 3 shows the structure of a Scan Flip-Flop. The multiplexer is added at the input of the flip-flop to select between functional input D and Scan-In (SI). The selection between D and SI is governed by the Scan Enable (SE) signal. Series of n-scan flip-flops are connected in form of a chain, which effectively acts as a shift register. The first flop of the scan chain is connected to the scan-in port and the last flop is connected to the scan-out port.

Scan operation involves three different operating stages: Scan-in, Scan-capture and Scan-out. Scan-in involves shifting in followed by loading all the flip-flops with an input vector. Once the sequence is loaded, one clock pulse (also called the capture pulse) is allowed to excite the combinatorial logic block and the output is captured at the second flop. The data is then shifted out and the signature is compared with the expected signature. Implementation of scan chain at 32nm node: A 1500-style die

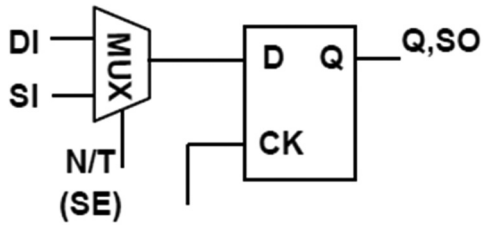

Figure 3*a*. Scan Flip Flop.

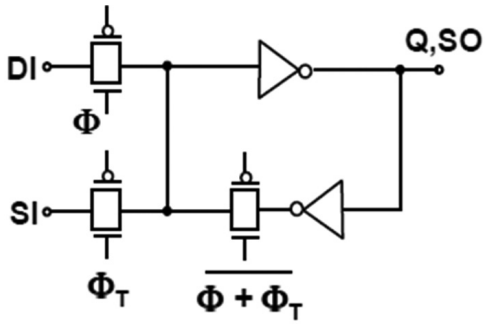

Figure 3*b*. MOS Transistor based scan flop.

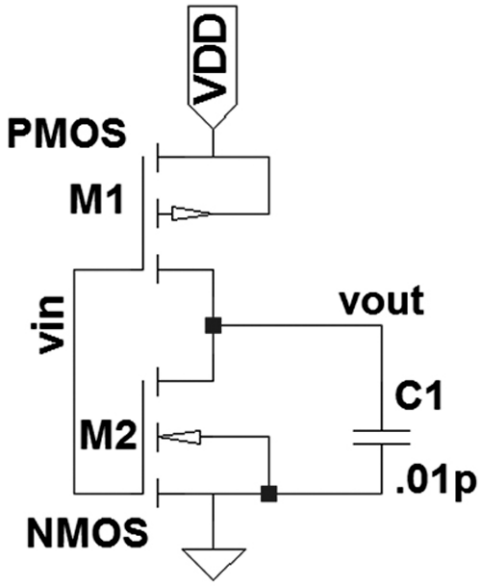

Figure 4*a*. CMOS Inverter Model.

wrapper with scan-based TSV tests has been proposed for post-bond external tests [25]. We introduce a scan flop, as shown in Figure 3 that is to be used in the mentioned 1500-style die wrapper. As seen at the block level in Figure 3a, the gated scan flop accepts either a functional input or a test input from the scan chain; the selection is made depending on operational mode. In our design, shown at the transistor level in Figure 3c, two cross-coupled inverters are used to store data. Transmission gates are inserted between the cross-coupled inverters and at the input (D) and output (Q) of the flop itself.

Figure 4 shows a CMOS inverter with capacitive load C1. Figure 2 shows the output voltage Vout of CMOS inverter for a falling input Vin using CMOS 32 nm PTM model [19], [26]. t_{50} is the time for the gate output voltage from the initial point to 50% VDD.

The gate propagation delay t_D is defined as the time interval from V_{in} = VDD/2 to V_{out} = VDD/2. From Figure 4*b*, gate delay can be represented as

$$t_D = t_{50} - t_{in} / 2 \quad (1)$$

Figure 4(c) shows the delay time $t_D$and the overshooting time

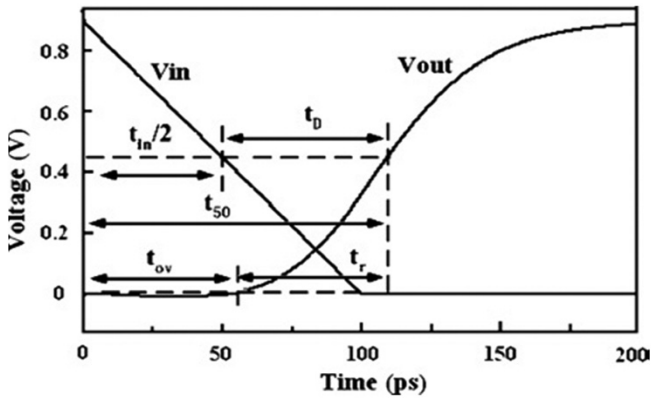

Figure 4*b*. CMOS Inverter response for a falling input [26].

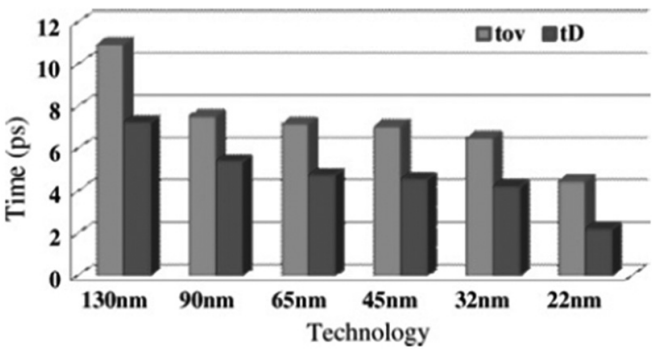

Figure 4*c*. Inverter response with various technologies [26].

t_{ov} for various process technologies from 130 nm to 22 nm with typical supply voltages. The transistor length L is the minimum feature size. The widths of all PMOS transistors Wp are ten

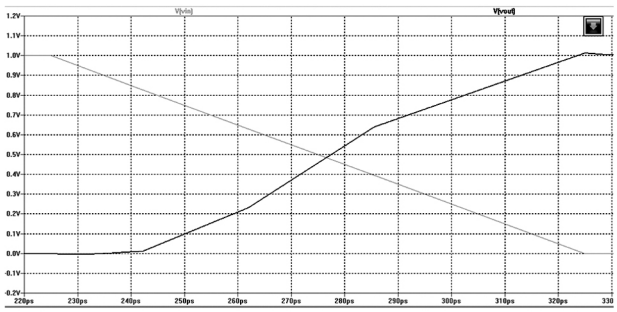

Figure 5*a*. Simulated Inverter response.

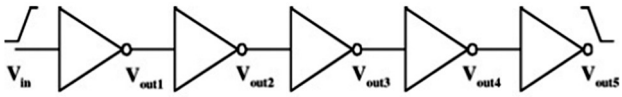

Figure 5*b*. Inverter chain.

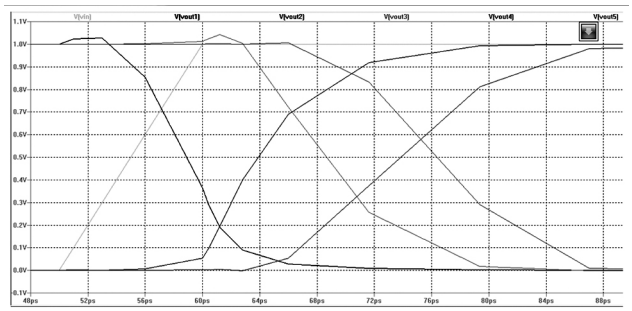

Figure 5*c*. Simulated response of inverter chain with 32 nm PTM model.

times of L while Wp is two times of Wn. The load capacitance C1 is 0.01 pF.

Results achieved by Zhangcai Huang *e. al.* [26] (shown in Figure 4*b* and Figure 4*c*) are verified by us on a SPICE tool using PTM 32 nm node technology. Figure 5*a* shows the CMOS inverter response for an input V_{in} with an approximate fall time of 100ps. The simulation results of the inverter achieved matches the results achieved in Figure 4*c* with an approximated error of 8% - 9%. These results are significant as scan flip flop shown in Figure 3*b* is implemented using the same CMOS inverter.

Currently, the use of delay models for performance cell based delay calculation has become an industry standard in practical .delay calculation tools. As cells are connected together by interconnect wires, the delay time of CMOS circuits between the input signal to output signal is just the sum of the delay time of each cell. To illustrate this, a chain of five inverters is used to observe the output waveform of each inverter as shown in Figure 5(b).

In Figure 5*c*., the delay time t_D of the inverter chain is measured to be 21.4 ps.

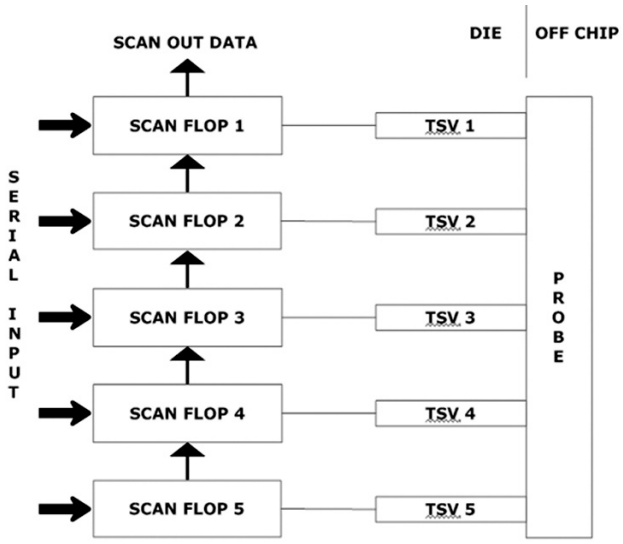

Figure 6*a*. TSV network model.

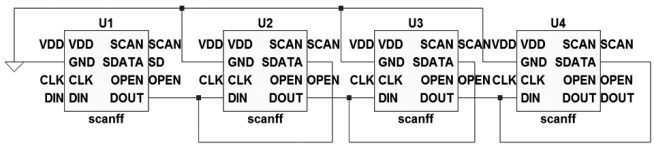

Figure 6*b*. SPICE implementation of Scan chain.

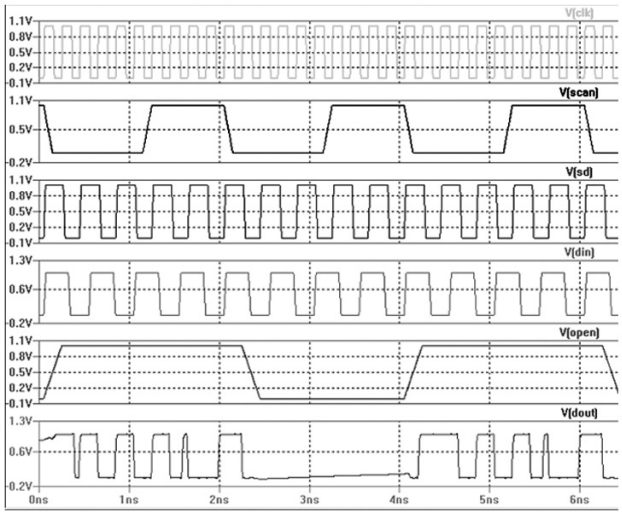

Figure 6*c*. Simulation of scan chain at 32nm node.

Cascading scan flops to form scan chain:

A TSV can be modeled as a wire with both a resistance and a capacitance. While a TSV may be manufactured from a number of different materials, copper is often used for metal layers and polysilicon may be a nonmetal alternative. The resistance of a TSV made from copper with a 2–5μm diameter and 5μm height is 80–200mΩ. For a polysilicon TSV with a 28–46μm diameter and 50μm height the resistance is 1.3–5.0Ω. The capacitance of a copper TSV with a 1–10μm diameter and 30–100μm height is 10–200fF. A probe needle makes contact with a number of TSVs at a time, as seen in Figure 6(a). The TSVs are connected to scan-flops, which are connected to form a scan chain [13]. Pre-bond testing of TSVs is difficult due to TSV pitch anddensity. Current probe technology using cantilever or vertical probes require a minimum pitch of 35μm, but TSVs have pitches of 4.4μm and spacings of 0.5μm. To address the aforementioned challenges, technique for pre-bond TSV testing that is compatible with current probe technology and leverages the on-die scan architecture that is used for post-bond testing. It utilizes many single probe needle tips, each to make contact with multiple TSVs, shorting them together to form a single network. This method requires probing, assuming that the die has already beenthinned and supported by a rigid platter (carrier) to prevent mechanical damage during probing. This method also allows for the concurrent testing of many TSVs to reduce overall test time.Furthermore, fewer probe needles are needed, which reduces the cost and complexity of probe equipment.

A method where all the scan-flops are initialized to known values is proposed. As shown in Figure 6*a*, scan flop 1 to 5 is initialized to logic HIGH or LOW. Multiple TSVs are shorted due to pitch limitations using current probe technology. We applied logic LOW or HIGH on the probe and read the values into the scan flop through the TSVs. A faulty TSV fails to update the new value into the scan flop and readily identified by shifting out the bit pattern.

Existing works deal with the post-bond test of TSVs by IEEE 1149.1 or IEEE 1500 test standards. Each TSV thus requires at least one register.

Figure 6(c) shows the simulation results achieved from the above scan chain. Clk frequency is taken at 5Ghz and scan signal is an input signal to the flop which puts the flop either in scan mode or conventional input mode. Scan flop selects multiplexed inputs (din) or serial data (sd) depending on the scan signal status (HIGH = scan mode, LOW = serial input mode). Open signal, determines whether the output Q floats or takes the value stored in the flip–flop.

IV. CONCLUSION

A cost-effective BIST scheme for testing TSVs of 3D ICs is presented in this paper. New on-chip measurement techniques targeted at 32nm ptm node technology that allows probing-based pre-bond testing of TSVs is introduced. Author demonstrated how these tests are applied to a network of TSVs, and presented LTSPICE simulation results to highlight the effectiveness of this approach.

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